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10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER
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ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	KIBROM K. GEBRESILASSIE	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4 and 5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4, and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on 07/17/2008.

2. Claims 4 and 5 are presented for examination.

Response to Arguments

3. Applicants are thanked for amendment/Remarks.

4. In previous office action, it was indicated that Figure 4 and Figure 5 have been ineligible. However, applicants have not reply for this issue. The objection is repeated in this Office action.

5. Applicant's argument relating to 101 rejection is not persuasive and the rejection is maintained. The claims as a whole are directed to verifying a system which the final steps is also verifying a system and therefore no tangible result, and thus no practical application is produce.

6. Applicant's argument relating to 112 rejection is persuasive and therefore the rejection is withdrawn.

7. Applicant's argument relating to art rejection is not persuasive and therefore the rejection is **maintained** for the following reasons.

a. Regarding 102(f) rejection: Applicant's have not shown how the emulator is transformed in their claimed invention to overcome the rejection. They indicated that the first and second circuitries are configured to realize and verify a first and a second system. However, this transformation is well known for many chip makers that use a hardware emulator as follows:

[0006] Many chip-makers now use a device called a hardware emulator to verify SOCs. A hardware emulator is a device with large amounts of logic and other circuitry with highly configurable connections. The connections can be configured so as to realize the design of the SOC. The

Therefore, the hardware emulator used by applicant's is still prior art. For this reason, the rejection is maintained.

b. Regarding 102(e) rejection: Applicants argued that the prior art of reference fails to disclose hardware emulator to realize the first system on chip and to realize the second system on another chip.

In response, the prior art of reference permits an SOC designer or programmer to test, evaluate, and/or debug the processor core (i.e. first system on chip) and/or the other core (i.e. second system on chip) using the emulation interface circuitry (i.e. hardware emulator) (See: [0039]).

Drawings

8. New corrected drawings in compliance with 37 CFR 1.121(d) is required in this application because the drawings are illegible (See, for example Figs. 4 and 5).

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 4, and 5 are rejected under 35 U.S.C. 101 as being directed to nonstatutory subject matter since the claims as a whole do not provide for a practical application and there is no physical transformation or a useful, tangible, and concrete final result.

Applicants Admission

11. Applicant's disclosure states as follows:

Prior art:

[0006] Many chip-makers now use a device called a hardware emulator to verify SOCs. A hardware emulator is a device with large amounts of logic and other circuitry with highly configurable connections. The connections can be configured so as to realize the design of the SOC. The design is usually described in a data structure. A script checks the capacity of the hardware emulator to determine whether the hardware emulator has sufficient logic and circuitry to realize the design described in the data structure. If the hardware emulator has sufficient capacity to realize the design described in the data structure, the script places the data structure in a top wrapper. The top wrapper parses the data structure describing the design and configures the hardware emulator to realize the design.

Compare to claimed invention:

[0023] FIGURE 2 is a block diagram of a hardware emulator configured in accordance with an embodiment of the present invention. The hardware emulator 200 comprises a sea of logic and other circuitry 205. The sea of logic and other circuitry 205 is configurable to realize a vast number of integrated circuits. The sea of logic and other circuitry can be divided into a plurality of portions 210.

[0026] The emulator 200 of FIGURE 2 can be configured by a computer system configured generally as described in FIGURE 3. An SOCs, SOC1...SOCn can be described in a data structure in a file. The file is parsed by a script. A script is a plurality of executable instructions stored in the memory of the computer system, or a removable memory, that parses the data structures, checks the capacity of the emulator 200, and creates another file, known as a top wrapper. The top wrapper is provided to the emulator and configures the emulator 200 in accordance with the SOCs described in the data structure.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (f) he did not himself invent the subject matter sought to be patented.

13. Claims 4, and 5 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter.

c. Applicant's admission establishes that applicant has invented a system of using a hardware emulator for verifying a plurality of systems of the prior art. Applicants have not disclosed inventing a hardware emulator system. As such, any claims directed to a system that facilities this system must be regarded as being invented by another.

d. These rejection may be overcome by evidence that applicant has somehow transformed the hardware emulator system of the prior art by some specialization. As currently disclosed, however, applicants' system of verifying using a hardware emulator merely uses the existing feature of the prior art.

e. Evidence that hardware emulator anticipates the invention of claims 4, and 5 is found in applicant's admission as explicitly recited in the disclosure of the invention.

14. Claims 4, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by US Publication No. 2004/0019827 issued to Rohfleisch et al.

15. As per Claims 1-3, Canceled.

16. As per Claim 4, Rohfleisch et al discloses a system for verifying a plurality of systems on a plurality of chips (such as *…SOC designer to test or evaluate and/or debug….*;See: [0039]), said system comprising:

a hardware emulator for verifying a first system on a chip and a second system on another chip (such as *…to test or evaluate and/or debug the processor core 102 (i.e. first system on another chip*) *and/or the other core (i.e. second system on chip) using the emulation interface circuitry...*See: [0039]) said hardware emulator comprising:

a first circuitry configured to realize and verify the a first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry system on the chip (such as *…to test or evaluate and/or debug the processor core 102 (i.e. second system on another chip*) *and/or the other core using the emulation interface circuitry...*See: [0039]); and

a second circuitry configured to realize and verify the a second system on another chip while the first circuit verifies verifying the first system on chip, the second circuitry directly connected to the first circuitry (such as *…to test or evaluate and/or debug the processor core 102 and/or the other core (i.e. second system on another chip*) *using the emulation interface circuitry...*See: [0039]).

17. As per Claim 5, Rohfleisch et al the system of claim 4, wherein the hardware emulator further comprises:

a first interface operable connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry (such as *…to test or evaluate and/or debug the processor core 102 and/or the other core using the emulation interface circuitry...*See: [0039]); and

a second interface operable connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (such as *…to test or evaluate and/or debug the processor core 102 and/or the other core using the emulation interface circuitry...*See: [0039]).

18. As per Claim 6-11, Cancelled.

Conclusion

19. All claims are rejected.

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. **Examiner Remarks:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. **Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well.** It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

22. **Examiner Request: In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on** for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

MPEP states:

"…with respect to newly added or amended claims, applicant should show support in the original disclosure for the new or amended claims. See MPEP § 714.02 and § 2163.06."

23. **Requests for Interview**: In accordance with 37 CFR 1.133(a)(3), requests for interview must be made in advance. Interview requests are to be made by telephone (571-272-8571) or FAX (571-273-8571). Applicants must provide a detailed agenda as to what will be discussed (generic statement such as "discuss §102 rejection" or "discuss rejections of claims 1-3" may be denied interview). The detail agenda along with any proposed amendments is to be written on a PTOL-413A or a custom form and should be faxed (or emailed, subject to MPEP 713.01.I / MPEP 502.03) to the Examiner at least 3 days prior to the scheduled interview. Interview requests submitted within amendments may be denied because the Examiner was not notified, in advance, of the Applicant Initiated Interview Request and due to time constraints may not be able to review the interview request to prior to the mailing of the next Office Action.

Communications

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is

571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kibrom K Gebresilassie/
Examiner, Art Unit 2128

/Alexander J Kosowski/
Primary Examiner, Art Unit 2128